REMARKS

Applicants respectfully request favorable reconsideration of the present application in view of the reasons that follow. Claims 1-11 are pending in the present application. Applicants believe that the present application is in condition for allowance.

Claims 1-11

In Section 2 of the Office Action, Claims 1-11 are rejected under 35 U.S.C. § 102(e) as being anticipated by published U.S. Patent Application No. 20040136210 (Oh). As an initial matter, it is noted that the published Oh application was filed on October 22, 2003, after the filing date (June 20, 2003) of the present application. Oh claims priority to a provisional application filed on October 23, 2002, which may or may not correspond to the disclosure of the published Oh application. Nonetheless, whether or not Oh is available as prior art, it is submitted that Oh fails to disclose, teach, or suggest the claimed invention as recited in Claims 1-11.

Claim 1 recites:

> the line-side converter including three gate controlled switching devices, each gate controlled switching device connected from each side thereof by anti-parallel oriented diodes to one of the input lines and each switching device connected by a diode to the DC link high line and by a diode to the DC link low line;

See, e.g., Figs 2 and 3 of the present application which show the anti-parallel connected diodes 46 and 47 and the diodes 48 and 49 that connect each switching device 45 to the high line and low line, respectively.

On page 2 of the Office Action, it is stated that Oh discloses "each gate controlled switching device connected from each side thereof by anti-parallel oriented diodes (114-1 to 114-6)." Oh, however, discloses "power diodes 114-1 ... 114-n [that] are coupled **across** power transistors 112." (page 2, paragraph [0020], emphasis added). Additionally, as shown in FIG. 1 of the Oh reference, a single diode couples across a single transistor. Thus, Oh fails to disclose, teach, or suggest "each gate controlled switching device connected from each side thereof by anti-parallel oriented diodes to one of the input lines" as recited by claim 1.

Oh also fails to meet the feature of "each switching device connected by a diode to the DC link high line and by a diode to the DC link low line". As shown in FIG. 1 of the Oh reference, no diode connects the power transistor 113 to the DC link high line. Additionally, no diode connects the power transistor 113 to the DC link low line. Thus, Oh fails to disclose, teach, or suggest "each switching device connected by a diode to the DC link high line and by a diode to the DC link low line" as recited by claim 1.

Claims 1 and 6 recite:

> a clamp circuit connected between the DC link high line and the DC link low line, the clamp circuit including a series connected diode and capacitor with the diode arranged to conduct current from the high DC link line to the low DC link line

The Office Action states that Oh discloses:

> a clamp circuit (120) connected between the DC link high line and the DC link low line (150), the clamp circuit including a series connected diode (124), capacitor (C1 and C2) and a switch (123) connected in parallel with the diode.

(Page 3, Office Action mailed March 4, 2005).

Oh does not disclose a clamp circuit. Oh discloses a **resonant DC link** 120 that includes an auxiliary power device 122. The auxiliary power device 122 of Oh includes "an auxiliary power diode 124 [that] can be coupled between the drain and the source of the MOS-FET." Oh additionally states that "[f]urther elements of resonant DC-link include a first capacitor C1, coupled in series with auxiliary power device 122, **an inductance Lr, coupled in parallel with auxiliary power device 122** and first capacitor C1." (page 2, paragraph [0027], FIG. 1, 2, 3A-3H, emphasis added). According to Oh, the resonant DC-link further includes a capacitor C2 in series with the inductance Lr and the auxiliary power device 122. (See page 2, paragraph [0027], FIG. 1, 2, 3A-3H). The operations of the resonant DC link 120 of Oh are different from a clamp circuit as evidenced by the series of circuit states, shown in FIGs. 3A-3H, in which the diode is not arranged "to conduct current from the high DC link line to the low DC link line." The diode conducts current through first capacitor C1 and inductance Lr and back to the high DC link line. (See page 3, paragraph

[0049], FIG. 3H). Thus, Oh fails to disclose, teach, or suggest "a clamp circuit ... including a series connected diode and capacitor with the diode arranged to conduct current from the high DC link line to the low DC link line."

Claim 6 additionally recites:

> a controller providing a control signal to the clamp switch to turn the clamp switch on to conduct current from the clamp capacitor to the DC link high line when the voltage across the clamp capacitor is above a threshold voltage that is greater than the normal peak-to-peak voltage across the input lines and to turn off the clamp switch when the voltage across the clamp capacitor is lower than the threshold voltage

Claim 11 similarly recites:

> when the voltage across the clamp capacitor is above a threshold that is higher than a normal peak-to-peak AC input voltage, turning on the clamp switch to discharge the clamp capacitor and conduct current through the switch to the load-side converter; and
>
> when the voltage across the clamp capacitor is below the threshold voltage, turning off the clamp switch and maintaining the clamp switch off as long as the voltage across the clamp capacitor is less than the threshold voltage

The Office Action states that Oh discloses

> a controller connectable to receive the AC voltages provided to the line-side converter and providing control signals to switch the switching devices of the load-side converter and the load-side converter with pulse width modulated control for AC output voltages on the output lines of the load-side converter.

(Page 3, Office Action mailed March 4, 2005).

Applicants respectfully traverse this statement. Oh discloses only that "resonant switch Qr is turned on at t=t0" (page 3, paragraph [0039]) and "[i]n Step 2 ... resonant switch Qr is turned off' (page , paragraph [0042]). Oh fails to disclose any controller at all. Additionally, Oh fails to disclose any control of the switch based on a voltage across the clamp capacitor. Thus, Oh fails to disclose, teach, or suggest "when the voltage across the

clamp capacitor is above a threshold that is higher than a normal peak-to-peak AC input voltage, turning on the clamp switch to discharge the clamp capacitor" and "when the voltage across the clamp capacitor is below the threshold voltage, turning off the clamp switch."

For the foregoing reasons, Oh fails to describe, suggest, or teach at least the features of "each gate controlled switching device connected from each side thereof by anti-parallel oriented diodes to one of the input lines," "each gate controlled switching device connected from each side thereof by anti-parallel oriented diodes to one of the input lines," a "diode arranged to conduct current from the high DC link line to the low DC link line," "when the voltage across the clamp capacitor is above a threshold that is higher than a normal peak-to-peak AC input voltage, turning on the clamp switch," and "when the voltage across the clamp capacitor is below the threshold voltage, turning off the clamp switch." As a result, Oh fails to disclose, suggest, or teach all of the limitations of claims 1, 6, and 11. Claims 2-5 depend from Claim 1. Claims 7-10 depend from Claim 6. These claims add further features to the independent claims and further distinguish from Oh. Therefore, Applicants respectfully request withdrawal of the rejection of claims 1-11.

Applicant believes that the present application is in condition for allowance. Favorable reconsideration of the application is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 50-2350. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-2350. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 50-2350.

Respectfully submitted,

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